# EXHIBIT 1

# High-Temperature Electronics—A Role for Wide Bandgap Semiconductors?

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*Invited Paper*

*It is increasingly recognized that semiconductor based electronics that can function at ambient temperatures higher than 150 °C without external cooling could greatly benefit a variety of important applications, especially in the automotive, aerospace, and energy production industries. The fact that wide bandgap semiconductors are capable of electronic functionality at much higher temperatures than silicon has partially fueled their development, particularly in the case of SiC. It appears unlikely that wide bandgap semiconductor devices will find much use in low-power transistor applications until the ambient temperature exceeds approximately 300 °C, as commercially available silicon and silicon-on-insulator technologies are already satisfying requirements for digital and analog very large scale integrated circuits in this temperature range. However, practical operation of silicon power devices at ambient temperatures above 200 °C appears problematic, as self-heating at higher power levels results in high internal junction temperatures and leakages. Thus, most electronic subsystems that simultaneously require high-temperature and high-power operation will necessarily be realized using wide bandgap devices, once the technology for realizing these devices become sufficiently developed that they become widely available. Technological challenges impeding the realization of beneficial wide bandgap high ambient temperature electronics, including material growth, contacts, and packaging, are briefly discussed.*

***Keywords*—Contacts, electronics, high temperature, metal–oxide–semiconductor field-effect transistor (MOSFET), packaging, power, semiconductors, sensors, SiC, silicon carbide, silicon-on-insulator (SOI), wide bandgap.**

## I. INTRODUCTION

The last three decades have witnessed an increasing proliferation of performance-enhancing electronics on a wide variety of automotive, aerospace, deep-well drilling, and other industrial systems. This proliferation continues to accelerate, largely driven by the availability of increasingly capable microelectronics coupled with the ever-growing demand for improved integrated system performance. The presence of high temperatures, well beyond the limits of conventional electronics, is inherent to the operation of many of these systems, particularly those involving fuel combustion, high-temperature manufacturing processes, and deep-well drilling.

When the environment temperature is too high, the performance-enhancing electronics presently used to beneficially monitor and/or control crucial hot-section subsystems must reside in cooler areas, either remotely located from the high-temperature region or actively cooled with air or liquid cooling medium pumped in from elsewhere. However, these thermal management approaches introduce additional overhead that can negatively offset the desired benefits of the electronics relative to overall system operation. The additional overhead, in the form of longer wires, more connectors, and/or cooling system plumbing, can add undesired size and weight to the system, as well as increased complexity, part count, and corresponding increased potential for failure [1]. These difficulties stand as major hinderances toward expanded use of electronics to directly improve hot-environment system performance. In aerospace systems, for example, weight, reliability, and system performance are all critical. The fact that increased electrical system wiring and connectors have become a significant operational reliability issue has been reinforced by highly public aerospace tragedies linked to degraded wiring, including TWA Flight 800 (near Long Island, NY, in 1996) and SwissAir Flight 111 (near Nova Scotia in 1998) with many fatalities. Even before these incidents, it was known that wiring and connector problems were a major cause of maintenance actions on aircraft jet engines [2].

Despite these difficulties, the drive to put even more electronics into aircraft and automobiles, including subsystems that monitor and control vital high-temperature areas

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of these vehicles, is unlikely to slow in the near future. In aircraft particularly, efforts are underway to increasingly replace hydraulically driven actuators and other subsystems with all-electric versions [3]. This is occurring in spite of the wire/connector reliability issues mentioned above because a mature electrical approach is believed to be inherently more reliable, more compact, lighter weight, and less maintenance-intensive than approaches that require fluids, pumps, and/or high-pressure/vacuum piping. High-temperature capability is vital to realizing improved electronic control in propulsion systems, where engine case temperatures can reach 600 °C [3], [4]. For further electronics to be beneficially incorporated into aerospace and other systems, it must be done in a manner that minimizes new wiring or other overhead that adversely impacts overall system reliability. It is generally accepted that reduced wiring in both aircraft and automobiles can be accomplished by a distributed network approach in which smart electronics are located where they are needed with only communication and power connections leaving the immediate area. This distributed electronics approach contrasts with the older approach of having electronics boxes consolidated at a central location on the vehicle controlling most system functions, each of which can require multiple sensor/control signal wires running throughout the airframe.

On modern aircraft, for example, it is not uncommon for a single-actuator subsystem control box to require 15–20 wire connections for the various sensing, control, power, and communication signals [1]. Considering the large number of electronic subsystems on a large passenger aircraft, overall wire weight and connector count can be drastically reduced when the electronics are integrated directly at the point of use, so that only power and communication interface wires leave the immediate subsystem. Over the longer term, completely wireless approaches are envisioned, wherein modules harvest their own power from the surrounding environment and distributed network data is exchanged by radio frequency, optical fiber, or other better medium than electrical wires. Elimination of wires is every bit as critical to telemetry systems that help guide deep-well drilling operations, which often extend 10 000–20 000 feet deep [5].

In the longer term, many of these modules may evolve into increasingly capable single-chip or multichip microelectromechanical systems (MEMS) that will be used to advance system performance. Arrays of advanced microsystems could augment or supplant existing subsystems and, in some cases, radically change the system design and implementation. For example, arrays of intelligent chips with microactuators have been proposed for adaptively changing the shape and flow of air on the skin of an aircraft or within the inside of a jet engine. To realize such a vision, electronics that provide self-contained functionality (power, communications, signal processing, microactuator control, etc.) at high ambient temperatures is required. Even for simpler microsystems envisioned within the next five to 10 years, such as sensors integrated with simple signal conditioning and/or wireless telemetry, there is already a recognized need for high ambient temperature functionality of both electrical (circuitry) and mechanical (transducer) aspects of the MEMS. High-temperature electronics functioning uncooled in/on the hot subsystem is vital to realizing this vision.

The economic benefits of high-temperature electronics to various systems is likely to be orders of magnitude greater than the total market for actual high-temperature electronics. The world market for high-temperature electronics in 2003 and 2008 is predicted to be near US $400 million and US $900 million, which is under a tenth of a percent of the total worldwide market for semiconductor electronics [6]. However, a mere handful of high-temperature electronics chips, perhaps purchased for a few hundred dollars, can enable many millions of dollars of increased capability to a very large system. For example, directional and compositional telemetry made possible by high-temperature electronics in a deep-well drilling operation can help prevent tens to hundreds of millions of dollars of loss in equipment and resources [5]. Similarly, sufficiently improved weight, fuel economy, and maintenance over the multidecade life of a commercial passenger aircraft would also translate into substantial operating cost savings. Even in a high-volume product like an automobile, the total value of all high-temperature electronics components will not likely be a large percentage of the total cost of a car [7]. Thus, high-temperature electronics can be characterized as a niche electronics market, albeit a fairly important one to many other products and systems that affect modern human life.

For the foreseeable future, wide bandgap semiconductors will be used for high ambient temperature electronics application needs that cannot be met by much more readily available semiconductor technologies. As is evident from almost all of the other papers in this Special Issue of the PROCEEDINGS OF THE IEEE, emerging wide bandgap semiconductor technology is far less developed than mature silicon-based semiconductor technology. Wide bandgap semiconductor materials and devices are more difficult and expensive to realize and less reproducible than well-established silicon. The added expense and development time needed to realize wide bandgap-based high-temperature electronics seems immediately justified only for those applications that are physically beyond the reach of conventional semiconductors.

## II. Operation of High-Temperature Semiconductor Electronic Devices

There are a number of factors both inside and outside the semiconductor that limit the high-temperature operation of semiconductor electronic devices and circuits. Proper understanding of these factors is crucial in determining which high-temperature applications can be met with mature technologies like silicon and silicon-on-insulator (SOI) versus which applications will be met with wide bandgap semiconductors. This section will briefly examine the main device physics limits of operating semiconductor devices at high temperature, with a particular emphasis placed on the most fundamental limits of silicon that wide bandgap semiconductors could be used to overcome.

### A. Intrinsic Carriers

The temperature effects within the semiconductor itself should be examined first because the fundamental physical limitations of silicon semiconductor operation are perhaps the strongest motivations for switching to wide bandgap semiconductors in higher temperature applications. As ambient temperature increases, semiconductor device characteristics degrade until they no longer provide sufficient functionality for desired circuit applications. One temperature degradation mechanism relates to the concentration of free carriers that governs device operation. Sufficient control of the local free carrier concentration is vital to operation of any semiconductor device and is primarily accomplished during device fabrication through the intentional introduction of doping impurities into various desired regions of the device. In silicon device technology at room temperature, the electron concentration of an n-type doped region is nearly equal to the concentration of n-type dopant introduced into the semiconductor during fabrication, while the hole carrier concentration of a p-type region is determined by the p-type impurity doping concentration. Depending upon the specific device, the lightest doped region of a silicon device usually falls somewhere between $10^{14}$ and $10^{17}$ atoms per cubic cm ($cm^{-3}$). However, dopant atoms are not the only source of electron and hole carriers in a semiconductor. Even if there were no doping present, every semiconductor would have a certain number of thermal electron and hole carriers present in the crystal. These carriers are referred to as intrinsic carriers because they are an intrinsic property of the semiconductor crystal at any given temperature. The concentration of these intrinsic carriers ($n_i$ in $cm^{-3}$) is exponentially dependent upon the temperature of the semiconductor [8], [9]

$$n_i = \sqrt{N_C N_V}\, e^{-E_G/2kT} \tag{1}$$

where $T$ is the temperature (in kelvin), $k$ is the Boltzmann constant ($8.62 \times 10^{-5}$ eV/K), $E_G$ is the energy bandgap of the semiconductor measured in electronvolts, and $N_C$ and $N_V$ are, respectively, the effective electron and hole density of states for the semiconductor ($cm^{-3}$). $E_G$, $N_C$, and $N_V$ are fundamental crystal properties that have substantially less temperature dependence compared to the explicit temperature exponential ($-E_G/2kT$) term of (1). The temperature dependence of intrinsic carrier concentration $n_i$ calculated from (1) is shown in Fig. 1 for silicon, 6H-SiC, and 2H-GaN (based on respective temperature-dependent material properties from [9]–[11]). At room temperature, the $n_i$ of silicon (1.1-eV bandgap) is around $10^{10}$ $cm^{-3}$, which is negligible compared to the $10^{14}$ to $10^{17}$ device doping levels mentioned above. However, as the ambient temperature is increased well beyond 300 °C, there can be as many or more intrinsic carriers present than dopant carriers in a given silicon device. Thus, the electrical conductivity of lighter doped regions of silicon devices become undesirably influenced by intrinsic carriers instead of the designed doping needed for proper electrical operation. From (1) and Fig. 1, it is easy to see that semiconductors with wide bandgaps (SiC and GaN) around 3 eV have much lower intrinsic carrier concentrations than silicon and, thus, do not run into intrinsic carrier conductivity difficulties until much higher temperatures, beyond 600 °C.

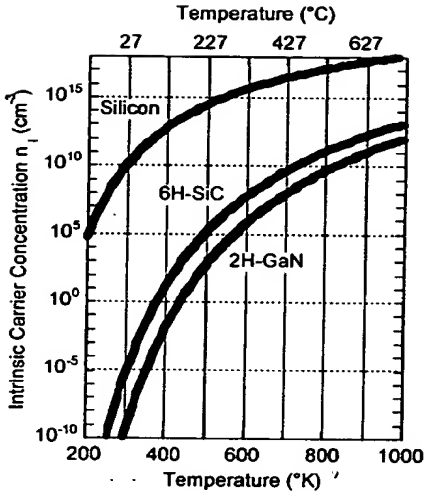


Fig. 1. Semiconductor intrinsic carrier concentration ($n_i$) versus temperature for silicon, 6H-SiC, and 2H-GaN.

### B. p-n Junction Leakage

The difference in intrinsic carrier concentration between silicon and the wide bandgap semiconductors perhaps becomes even more important when one considers the fundamental current–voltage ($I$–$V$) properties of rectifying junctions in semiconductor devices. Simple rectifying junctions typically conduct current when a forward bias voltage is applied and prevent current flow when the opposite polarity (reverse bias) voltage is applied. These junctions are a fundamental basis of almost all semiconductor electronic devices. Such junctions consist of intimate junctions of n-type (negatively charged electron carriers) and p-type (positively charged hole carriers) regions to form a p-n junction within a semiconductor crystal [9], [12]. A scan of transistor cross sections in semiconductor device textbooks reveals not only that almost all transistor structures are at least partially composed of p-n junctions, but also that their functional performance is largely dependent on the good rectification properties of each such junction in the device [9]. For example, in most solid-state power diodes and transistors, desired off-state blocking of current flow at high voltages takes place at a simple reverse-biased p-n junction [13]. In almost all circuit applications, the leakage currents of p-n junctions should be kept negligible with respect to the desired signal currents. The physics of the p-n junction with its depletion region (named because mobile carriers are "depleted" at the junction) are well detailed in semiconductor device textbooks. The $I$–$V$ behavior of a p-n junction diode (for the case where the p-type doping is much larger than the n-type doping) is approximately [9], [12]

$$I \cong qAn_i \cdot \left[\frac{n_i}{N_D}\sqrt{\frac{D_P}{\tau}}\left(e^{qV_A/kT}-1\right)+\frac{W}{2\tau}\left(e^{qV_A/2kT}-1\right)\right] \tag{2}$$

where $A$ is the area of the p-n junction ($cm^2$), $V_A$ is the voltage applied to the diode (volts), $N_D$ is the n-type doping density ($cm^{-3}$), $W$ is the width of the junction depletion region (centimeters) at applied voltage $V_A$, $D_P$ is the hole diffusion constant ($cm^2/s$), and $\tau$ is the effective minority carrier lifetime (seconds). The first exponential term in (2) is minority carrier diffusion current, while the second exponential term arises from thermal generation or recombination of carriers that occurs in the depletion region of a biased diode. For negative $V_A$ (i.e., reverse bias) greater than a few tenths of a volt at temperatures below 1000 °C, the exponential terms become insignificant compared to $-1$, so that (2) simplifies to

$$I \cong -qAn_i \left[ \frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right]. \tag{3}$$

From (3), it is easy to see that the leakage current of a reverse-biased p-n junction is fundamentally tied to the intrinsic carrier concentration $n_i$ of the semiconductor. The exponential temperature dependence of $n_i$ [via (1)] dominates the much smaller temperature variation of the other terms in (3). Thus, reverse-bias junction leakage currents harmful to device and circuit operation increase exponentially with temperature. Because wide bandgap semiconductors have much lower intrinsic carrier concentrations ($n_i$) than silicon (see Fig. 1), the leakage currents are orders of magnitude smaller than silicon, provided that junctions are realized in crystals of adequate structural quality. Therefore, wide bandgap semiconductor devices are capable of much higher temperature operation with respect to this fundamental limitation in excess of 600 °C.

### C. Thermionic Leakage

Another fundamental leakage mechanism in devices is the transport of carriers that gain sufficient energy to go over or tunnel through an energy barrier in a device structure. This process, called emission, increases with temperature as carriers gain more thermal energy. Manifested in a rectifying metal–semiconductor diode (i.e., Schottky barrier contact), the current due to carrier emission as a function of temperature and applied voltage is approximated by [14]

$$I \cong AK^*T^2 e^{-q\Phi_B/kT}(e^{qV_A/kT} - 1) \tag{4}$$

where $\Phi_B$ is the effective potential barrier height (i.e., Schottky barrier height) of the junction (in electronvolts) and $K^*$ is the effective Richardson constant of the semiconductor. For appreciable reverse biases ($V_A < -0.2$ V), the reverse-bias leakage current calculated from (4) simplifies to

$$I \cong -AK^*T^2 e^{-q\Phi_B/kT}. \tag{5}$$

From (5), it is easy to see that carrier emission leakage current is exponentially reduced as the effective potential barrier height $\Phi_B$ is increased. While $\Phi_B$ can depend on the metal, the semiconductor, and the junction formation process, barrier heights no larger than the semiconductor bandgap can be obtained. Practical Schottky barrier contacts based on most semiconductors have effective barrier heights usually less than three quarters of the bandgap energy. Thus, while silicon (1.1-eV bandgap) Schottky barrier heights are practically confined to less than 0.9 V, barrier heights over twice as large can be realized in wide bandgap semiconductors (~3-eV bandgaps), which reduces the junction leakage current at any given temperature by at least several orders of magnitude. This enables the realization of high-voltage and high-temperature wide bandgap Schottky power rectifiers not possible with conventional semiconductors.

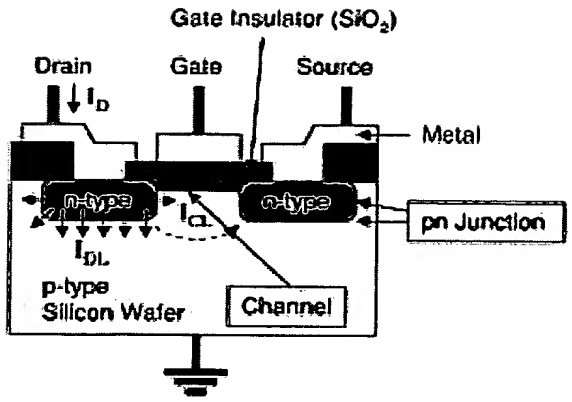


Fig. 2. Schematic cross section of an n-channel silicon MOSFET. The n-type doped source and drain regions form rectifying junctions with the p-type substrate. Current flow between the source and drain is modulated by the gate voltage that determines the density of electrons in an inversion channel in the semiconductor just under the oxide. The turnoff characteristics of the device are primarily governed by temperature dependent subthreshold channel leakage current ($I_{CL}$) and drain-to-substrate reverse leakage current ($I_{DL}$).

### D. Carrier Mobility

As temperature is increased well above room temperature, the ability of carriers to move through a semiconductor crystal is decreased. This arises because atoms in the crystal lattice have more thermal vibrational energy that results in more collisions with carriers moving through the crystal in response to an electric field. The resulting decrease in carrier mobility with temperature due to lattice scattering reduces the amount of current that a diode or transistor can carry. In general, the increase in semiconductor device resistance with temperature follows a $T^x$ power law behavior, where $x$ is usually between 1.5 and 2.5 for most semiconductors well above room temperature where lattice scattering is dominant, including silicon and wide bandgap semiconductors [9].

### E. Temperature Performance of Bulk Silicon Metal–Oxide–Semiconductor Field-Effect Transistors

The vast majority of semiconductor transistors fabricated and in use today are silicon-based metal–oxide–semiconductor field-effect transistor (MOSFETs), with n- and p-channel MOSFETs integrated on the same chip into complementary MOS (CMOS) circuits. It is, therefore, useful to briefly examine the specific impact of the basic mechanisms discussed above on the electrical performance of an n-channel MOSFET device, whose schematic cross section is depicted in Fig. 2. The source and drain regions of this device are formed through the intentional patterned

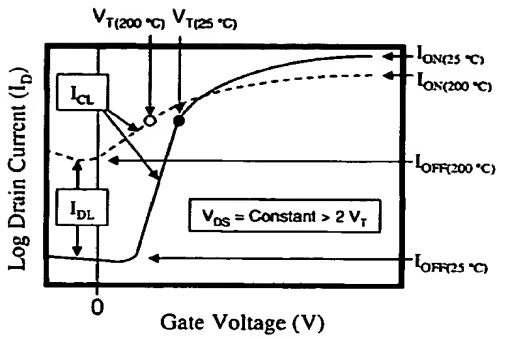


Fig. 3. Generalized drain current ($I_D$ on a logarithmic scale) versus gate voltage ($V_G$) characteristics of an n-channel silicon illustrating the degradation of electrical behavior with increasing temperature. As temperature is increased from 25 °C to 200 °C with a fixed drain-to-source voltage ($V_{DS} > 2V_T$), the on-state current ($I_{ON}$), and current gain ($dI/dV_G$) decreases due to decreased electron mobility at high temperature. Threshold voltage shifts to a slightly more negative voltage, while the off-state current ($I_{OFF}$) increases exponentially with temperature.

diffusion or implantation of n-type doping impurities into the p-type bulk crystal and an insulator (usually $SiO_2$) is formed between the gate terminal and the semiconducting channel. Fig. 3 shows the general behavior of MOSFET drain current ($I_D$) as a function of applied gate voltage ($V_G$) for a constant applied drain-to-source voltage ($V_{DS}$) at two different ambient temperatures. The drain-current axis of Fig. 3 is given on logarithmic scale, so that off-state current (typically nanoamperes or less at room temperature) temperature behavior can be plotted and compared with on-state current temperature behavior. When a voltage is applied between the source and drain contacts, current flow takes place by transport of electrons in the channel just on the semiconductor side of the oxide/semiconductor interface. The number (i.e., density) of electron carriers in the channel is controlled by the voltage applied to the gate terminal. When the gate is biased at a voltage such that essentially there are no electron carriers in the channel (i.e., below the "threshold voltage" $V_T$), current flow between the source and the drain is effectively turned off. When the gate is biased such that many electron carriers populate the channel (i.e., above the threshold voltage $V_T$), the device is turned on to carry an abundance of current ($I_{ON}$) between the source and drain terminals. In the n-channel MOSFET device, the n-doped source and drain regions are kept at zero or positive voltage with respect to the grounded p-type substrate, so that the p-n junctions in Fig. 2 are reverse-biased to nominally prevent current flow outside of the gate-voltage-modulated channel.

Starting at the right-hand side of Fig. 3, when strong positive biases are applied to both the gate ($V_G > V_T$ to attract electron carriers into the channel) and drain ($V_D > V_G - V_T$), a large on-state electron current flows through the channel approximated by [15]

$$I_D = \mu C_O \frac{W_G}{L_G} (V_G - V_T)^2 \qquad (6)$$

where $W_G$ is the transistor gatewidth (centimeters), $L_G$ is the transistor gatelength (centimeters), $\mu$ is the effective electron channel mobility ($cm^2$/V-sec), and $C_O$ is the insulator capacitance per unit gate area ($F/cm^2$). For any fixed gate voltage above threshold (i.e., $V_G > V_T$), the on-state current and transistor gain ($dI_D/dV_G$) is larger at room temperature than 200 °C due to the decrease in carrier (i.e., channel electron) mobility ($\mu$) with temperature. As the gate voltage is decreased in Fig. 3, the channel current in (6) decreases because there are fewer electrons attracted into the channel to carry current. The threshold voltage $V_T$ of the device decreases slightly with temperature [9]. As the gate voltage is decreased below threshold (i.e., $V_G < V_T$), electrons are repelled from the oxide-semiconductor interface effectively turning off current flow in the channel. At this point a parasitic flow of electrons carries a "subthreshold" channel leakage current (labeled $I_{CL}$ in Figs. 2 and 3) via carrier emission over the potential barrier between the source and drain created by the applied gate bias. As gate bias is decreased further below threshold, the height of the channel potential barrier to electrons correspondingly increases. The increasing channel potential barrier with decreasing applied gate voltage causes an exponential decrease in subthreshold emission current $I_{CL}$, very much analogous to increasing $\Phi_B$ in (5). This exponential current drop with decreasing gate voltage appears linear on the logarithmic current scale of Fig. 3 and is often characterized by a subthreshold slope parameter given in volts per decade. The fact that the subthreshold slope degrades (i.e., it takes more change in gate voltage to get channel leakage current $I_{CL}$ to drop by a decade) is consistent with (5) in that a larger change in $\Phi_B$ is needed at higher temperature to reduce the leakage current by a factor of ten. It is important to note that the drive to increase chip speed and transistor count has driven transistor gate length ($L_G$) well into the submicrometer regime for digital and analog integrated circuits (ICs). At this small dimension, the drain is physically located close enough to the source that applied drain voltage effectively lowers the height of the channel potential barrier all the way to the source side of the channel [9]. Therefore, subthreshold leakage $I_{CL}$ is worse in short-channel (i.e., submicrometer gate length) MOSFETs that are needed for very large scale integrated (VLSI) and ultralarge scale ICs.

The drop in drain current via $I_{CL}$ continues with decreasing gate voltage until it reaches the reverse-bias leakage current $I_{DL}$ associated with the drain-to-substrate p-n junction diode. The minimum off-state current ($I_{OFF}$) in a MOSFET is, therefore, limited by the reverse leakage of this diode. As discussed previously with respect to (1)–(3), this leakage current scales with the exponential temperature dependence of intrinsic carrier concentration $n_i$, which rapidly becomes an operational difficulty as ambient temperatures are increased above 150 °C in silicon devices. The high-temperature leakage current inherent to operation of silicon above 150°C can lead to $I_{ON}/I_{OFF}$ ratios that are unacceptable for many circuits. MOSFET-based circuits function well in large part because high on-state current leads to higher frequency circuits, while low off-state leakage enables low power dissipation so that millions of transistors on the same chip will not overheat. In addition, low off-state current also serves to

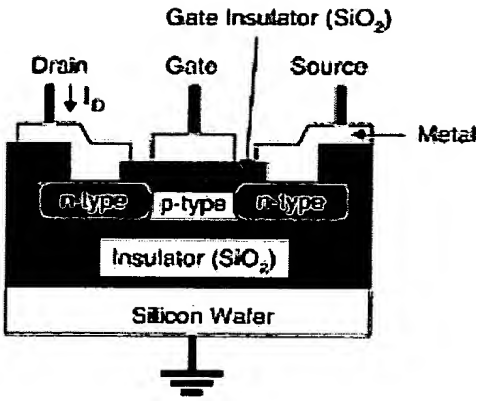


**Fig. 4.** Schematic cross section of an n-channel SOI MOSFET. Buried insulator greatly decreases the leakage area associated with the drain and source p-n junction diodes, which helps enable higher temperature operation.

minimize undesired interdevice signal crosstalk and latchup failure. While the specifics may be somewhat different for other silicon device topologies, such as bipolar junction transistors (BJTs), the basic argument of excessive junction leakage leading to circuit failure is common to all silicon technologies operating at too high ambient temperature [16]. Because reverse leakages are many orders of magnitude less in a wide bandgap semiconductor, acceptably large transistor on-to-off ratios can be maintained up to much higher operating temperatures, theoretically in excess of 600 °C.

The off-state current minimum ($I_{OFF}$ in Fig. 3) of the MOSFET increases with temperature by orders of magnitude, while the on-state current maximum ($I_{ON}$) decreases much less dramatically. Because the minimum off-state current is limited by the leakage of the drain-to-substrate p-n diode, any method that decreases this leakage to improve off-state current at higher temperatures would expand the peak temperature at which the silicon-based MOSFETs could provide adequate circuit functionality.

### *F. SOI Technology*

Silicon MOSFETs with improved off-state current for higher temperature operation are realized with the SOI approach schematically depicted in Fig. 4. Compared to Fig. 2, the Fig. 4 SOI approach eliminates the p-n junction area associated with the horizontal bottom and one vertical side associated with each n-doped region. Because the vertical depth dimensions of MOSFET n-doped source/drain regions are roughly an order of magnitude smaller than the lateral dimensions, the leakage area of the junction is decreased by around a factor of 100. The presence of the underlying insulator also reduces off-state source to drain carrier emission leakage ($I_{CL}$) that physically occurs deeper in the p-type substrate of conventional MOSFETs. This enables SOI MOSFET-based circuits to successfully operate in the 200 °C–300 °C temperature range, which is generally beyond the operating realm of conventional bulk silicon MOSFETs. Other device structures and circuits, such as bipolar transistors, have also been implemented using SOI methodology [17]. One drawback of the SOI approach is that it has been somewhat more difficult to implement than bulk silicon technology. The economic realization of uniform high-quality silicon on top of high-quality insulator on a mass-produced wafer scale has been a nontrivial technical challenge more difficult than manufacturing bulk silicon wafers.

Significant technology and reliability challenges outside the semiconductor have been successfully overcome in SOI. For example, in order to implement a MOSFET that can operate at 200 °C–300 °C for long time periods, the gate insulator (see Fig. 4) must maintain good insulating and interfacial properties under high-temperature and high electric field stress. An important failure mechanism associated with silicon MOSFETs at high temperature is the degradation of the gate oxide that occurs when carriers enter the oxide from the semiconductor. When there is sufficient temperature and applied electric field, mobile carriers (electrons and holes) can enter and propagate through the gate oxide, leaving behind damage and trapped charge in the oxide as well as at the oxide/semiconductor interface. This process results in degradation of gate-insulator electronic properties, including undesirably shifting the MOSFET threshold voltage $V_T$ that could result in circuit degradation and failure [9]. Therefore, one consideration in designing silicon MOSFETs is ensuring that electric fields in the oxide are low enough that significant insulator degradation is avoided for the desired operating voltage, temperature, and lifetime of the device. Another failure mechanism that increases with temperature is electromigration in which current flow over time gradually displaces microscopic metal traces on an IC, eventually leading to failure [18]. By overdesigning suitable interconnect and contact materials with large cross-sectional areas to minimize current density, sufficiently reliable operation has been obtained for 200 °C–300 °C SOI ICs [19]. With proper materials selection, chip packages, connectors, and circuit boards suitable for 200 °C–300 °C operation have also been developed [20].

The SOI approach is now well commercialized for a variety of applications, including high-temperature electronics. A variety of SOI-based ICs and foundry services rated to 225 °C are commercially available for low-power digital and analog applications. With appropriate operational lifetime derating, many of these circuits can operate at 300 °C. Given the ability of SOI to meet the need for low-power circuits at temperatures up to 300 °C, it appears that other semiconductors (such as wide bandgaps) are not needed for this application space. The added development and implementation expense of other semiconductors only appears justified where operation beyond the capability of SOI is required. Thus, it is unlikely that wide bandgap semiconductors will find much use in low-power circuits until the ambient application temperature exceeds 300 °C.

It is worth noting that gallium arsenide (GaAs) and related alloy (e.g., AlGaAs) device technologies, which are commercialized to a much smaller degree than silicon, are candidates for extending high-temperature operation somewhat (perhaps an additional 100 °C) beyond 300 °C. An excellent summary of issues facing high-temperature

electronics implementation with GaAs/AlGaAs technology is contained in [16]. While short-term electronic operation of devices at temperatures as high as 500 °C has been achieved [21]–[23], long-term operation of these electronics appreciably beyond capability of SOI remains undemonstrated. Thus, there has been little use of GaAs in high ambient temperature applications.

### G. High-Temperature Power Devices

Silicon-based power devices have long been used for repetitive switching (typically at kilohertz frequencies or less) inside power management and motor control circuits. The large benefits that wide bandgap devices promise to high-power switching applications at ambients below 150 °C are addressed in [60]–[62]. However, it is important to note that high ambient temperature versions of power management circuits are needed to realize many of the system improvements discussed in the introduction. While commercial SOI will be favored for most low-power high-temperature applications to 300 °C, there are important reasons why it is not nearly as suited to provide high-power functionality at this ambient temperature. When large operating currents are flowing through a power semiconductor device, some of that power is always lost to semiconductor resistance within the device itself. Also, when a power semiconductor device switches on and off there is almost always a brief period of time (on the order of a microsecond, usually associated with movement of charge in the device) where both the current and voltage are large, which leads to large instantaneous dynamic power dissipation [9], [13]. This dynamic power dissipation becomes significant and, in some cases, dominant when the devices are switched at higher switching frequencies necessary to minimize power converter size [24], [25]. Also, off-state leakage current that flows while the device is blocking a high voltage at high temperature can also lead to undesired power dissipation. All of these power dissipations can significantly raise the temperature inside a device (often referred to as the peak junction temperature) well beyond the ambient temperature. Making matters worse is the fact that all three of these power dissipations tend to increase with junction temperature, resulting in an undesired positive feedback loop of increasing temperature and power dissipation. Even for room temperature ambient operation, proper thermal management (i.e., cooling in the form of air conditioning, fans, heatsinks, etc.) is a key design consideration in many of today's solid-state power systems.

When the ambient temperature starts to exceed 200 °C, it becomes extremely problematic to ensure safely cool internal junction temperatures in silicon high-power devices, especially those rated to block hundreds or thousands of volts. High-power devices are typically operated at much higher voltages and electric fields, where reverse-bias leakage currents are significantly larger than in signal level devices. As discussed in [9], [13], [60], and [61], much lighter doping ($N_D$) and much larger depletion width ($W$) are required for a junction to block higher voltage. For silicon junctions, it can be shown from some mathematical manipulations of equations in [13] that the junction doping $N_D$ required for blocking voltage $V_B$ must be less than

$$N_D < 2 \times 10^{18}(V_B)^{-4/3} \tag{7}$$

and the depletion width $W$ must be greater than

$$W > 1 \times 10^{-6}(V_B)^{7/6} \tag{8}$$

even in the case where punchthrough structures aimed at minimizing $W$ are employed. Furthermore, larger junction area ($A$) is required for a device to support high on-state current. These factors combine undesirably to increase the reverse leakage current as described by (3), so that unacceptable leakage currents are reached at significantly lower junction temperatures in high-power devices than in low-power devices. Therefore, the off-state leakage currents generally reach unacceptably high levels at lower temperatures than for low-voltage low-power devices implemented in the same basic technology. The fact that junction heat energy removal is a function of temperature difference between the junction and the surrounding ambient makes it very difficult to passively radiate sufficient dissipated energy to keep silicon high-power junctions sufficiently cool for reliable operation in high ambient temperature environments. For lateral SOI power devices, the heat removal problem is exacerbated by the poor thermal conductivity of the buried oxide insulator. SOI also precludes the use of vertical device geometries wherein one of the high current contacts can efficiently reside on the semiconductor wafer backside. While a variety of novel power devices are being implemented in SOI [26], this approach cannot raise the silicon power device ambient temperature ceiling to the degree that it can increase the ambient temperature ceiling for low-power silicon devices.

The combination of necessary material properties required to meet demanding high-temperature and high-power application requirements can only be found in wide bandgap semiconductors. The inherent ability of wide bandgap semiconductor junctions to properly rectify with low reverse leakage at junction temperatures as high as 600 °C enables power-device operation at higher ambient temperatures [27]. As described in [60] and [61], superior power switching properties of wide bandgap devices are also present at room temperature ambient. Therefore, if remaining technical challenges can be overcome, wide bandgap semiconductors are likely to play a critical role in realizing high-power electronics beyond the capability of silicon at all temperatures.

## III. Wide Bandgap High-Temperature Technology Challenges

In light of the preceding discussion of semiconductor device high-temperature capabilities, it is useful to look at some specific applications. Table 1 outlines some of the better known high-temperature electronics application areas [6], [7], [16], [19] and speculates (based on the preceding discussion) on which of these areas wide bandgap semiconductors might play a significant role in the future once they have become sufficiently developed. Given the relevance of power level to the choice between silicon and wide bandgap devices for an application, Table 1 contains a chip power

Table 1
Semiconductor Technologies for Some Selected High-Temperature Electronics Applications [6], [7], [16], [19]

| High Temperature Electronics Application | Peak Ambient | Chip Power | Current Technology | Future Technology |
|---|---|---|---|---|
| Automotive | | | | |
| Engine Control Electronics | 150 °C | < 1 kW | BS & SOI | BS & SOI |
| On-cylinder & Exhaust Pipe | 600 °C | < 1 kW | NA | WBG |
| Electric Suspension & Brakes | 250 °C | > 10 kW | BS | WBG |
| Electric/Hybrid Vehicle PMAD | 150 °C | > 10 kW | BS | WBG |
| Turbine Engine | | | | |
| Sensors, Telemetry, Control | 300 °C | < 1 kW | BS & SOI | SOI & WBG |
| | 600 °C | < 1 kW | NA | WBG |
| Electric Actuation | 150 °C | > 10 kW | BS & SOI | WBG |
| | 600 °C | > 10 kW | NA | WBG |
| Spacecraft | | | | |
| Power Management | 150 °C | > 1 kW | BS & SOI | WBG |
| | 300 °C | > 10 kW | NA | WBG |
| Venus & Mercury Exploration | 550 °C | ~ 1 kW | NA | WBG |
| Industrial | | | | |
| High Temperature Processing | 300 °C | < 1 kW | SOI | SOI |
| | 600 °C | < 1 kW | NA | WBG |
| Deep-Well Drilling Telemetry | | | | |
| Oil and Gas | 300 °C | < 1 kW | SOI | SOI & WBG |
| Geothermal | 600 °C | < 1 kW | NA | WBG |

BS = bulk silicon, SOI = SOI, NA = not presently available, WBG = wide bandgap.

column that roughly approximates the semiconductor device power requirements. The chip power is not a true measure of the average power dissipated by a device or chip, but is instead defined as the maximum blocking voltage multiplied by the maximum operating current.

The preceding sections have focused on how wide bandgap semiconductors expand the temperature limits of electronic devices beyond the limits of silicon technology. However, the ability of wide bandgap semiconductors to electrically function at high temperatures will be of little practical use until important wide bandgap technology challenges are surmounted. This section briefly discusses major technical challenges that wide bandgap semiconductors must overcome in order to enable beneficial high-temperature electronic circuits.

### A. Materials

SiC-based and III-nitride (III-N)-based devices (primarily GaN) are the most developed wide bandgap semiconductors. As discussed in [63] and [64], difficult crystal growth and material quality challenges remain to be surmounted in both these materials. Mass-produced single-crystal SiC wafers have been commercially available for more than a decade, while III-N device crystals have mostly been grown by heteroepitaxy on foreign substrates like sapphire and SiC. SiC device crystals have traditionally had orders of magnitude fewer crystal dislocation defects than GaN. Thus, it is not surprising that more wide bandgap research aimed at high ambient temperature devices has been carried out on SiC than GaN. As a result, SiC is more advanced in some important technology areas than the III-Ns, such as better control of crystal impurities needed to realize electronic devices. Dopant impurity diffusion is practically nonexistent in the wide bandgaps for envisioned operating temperatures (< 600 °C), but elements that interfere with electrical properties (such as hydrogen) can undesirably be activated at this temperature in the III-N crystals [11]. Crystal dislocation defects present in both SiC and GaN adversely affect the $I$–$V$ properties of p-n junctions, causing leakage currents larger than those predicted by (3) [28]–[30]. Depending upon the device application and the specific type and density of the defects, the junction leakage can become so severe that it effectively prevents advantageous high-temperature operation of wide bandgap devices. The material defects also have a greater impact on high-power devices due to the high electric field and large junction area. For example, SiC power device blocking voltage is known to degrade as increasing device area encompasses more crystal defects [31], [32]. Structural crystal defects affect low-power devices to a lesser degree because they are operated at lower electric fields and have smaller junction areas. Additional nonidealities in wide bandgap device layers, such as variations in layer doping and thickness across the wafer and surface morphological defects, can also harm device capability. Continued improvements in crystal growth and material quality are necessary for the successful realization of wide bandgap high-temperature electronics.

Despite nonoptimal crystals, low-power prototype SiC electronic circuits [33]–[35] as well as III-N devices [11] have demonstrated operation in the 300 °C–600 °C temperature range. However, none of these devices or circuits were able to operate at high temperature for time periods sufficient for most applications. Achieving long-term reliable operation is one of the primary obstacles to realizing useful 300 °C–600 °C wide bandgap devices and circuits. The reliability challenge of long-term functionality at 300 °C–600 °C could demand more radical technological modifications than were necessary for the transformation from silicon to high-temperature (200 °C–300 °C) SOI.

### B. Contacts

All useful semiconductor electronics require conductive signal paths in and out of each device as well as conductive interconnects to carry signals between devices on the same chip and to external circuit elements that reside offchip. The high-temperature functionality of wide bandgap semiconductor devices is useless without ohmic contacts and interconnects that are also capable of operation under the same conditions. The durability and reliability of metal–semiconductor contacts and interconnects is presently a primary factor limiting the operational high-temperature limits of wide bandgap electronic devices and circuits. Contact metallizations for the 300 °C–600 °C temperature range presents fundamental reliability challenges that must be overcome. Although III-N-based optoelectronics have found widespread application at room temperature, contact degradation from self-heating generated during operation is partially recognized as a limiting factor to the performance and long-term reliability of these devices [11]. Depending upon the high-temperature device structure, ohmic (and Schottky, where necessary) contacts to n-and p-type layers are required to be thermally stable during the operational life of the device. Consistent with the relative status of crystal growth technology, SiC high-temperature contacts have generally demonstrated more advanced high-temperature capability than III-N contacts. Due in part to differences between donor and acceptor dopant ionization energies, significantly more conductive n-type doping layers can be obtained than p-type layers in both SiC and III-N semiconductors, which in turn has enabled n-type ohmic contacts to become more mature with better performance than p-type contacts.

Earlier works by researchers in contacts to SiC-based devices had, with great success, focused primarily in understanding the reaction kinetics and electrical characteristics at the metal/SiC interface. A comprehensive review of these efforts for SiC was given by Porter *et al.* [36]. Further progress was made at achieving contact thermal stability by investigating diffusion barriers in multilayer metallization systems [37], [38]. Development of high-temperature III-N contacts has generally followed a similar progression. A significant common denominator in these previous results is the fact that high-temperature testing was conducted in either a controlled inert ambient, such as pure nitrogen or argon, or vacuum environments. The challenges of attaining perfect hermetic electronics packaging for the 300 °C–600 °C temperature range are briefly discussed in the next section. Unless the goal of these efforts is to develop hermetically sealed packaging to protect the contacts, it seems more practical that the true test of contact stability at high temperature should be based on atmospheric exposure. Contacts that are stable in high-temperature air ambient will require simpler and less expensive packaging.

There has been substantial recent progress toward realizing high-temperature ohmic contacts to SiC that are stable in air at high ambient temperatures. For example, TiW-based contacts with aluminum interconnect and wiring endured over 500-h heat treatment at 400 °C in air [39]. More recently, a Ti/$TaSi_2$/Pt multilayer contact to n-type SiC recently demonstrated stable ohmic properties over the course of 1000 h of annealing at 600 °C in air [40], [41]. Lateral oxidation encroaching from the edge of the contact pattern was noted to degrade the contact by the end of the anneal. However, this failure mechanism can be greatly minimized with conventional dielectric passivation (e.g., $SiO_2$ or $Si_3N_4$) that was not used in this experiment. Further progress is necessary before similar results can be obtained for p-type SiC. Given the excessive difficulties of obtaining highly conductive p-type III-N layers, the realization of highly stable contacts to this material will likely prove a most difficult challenge [11]. In part because of the difficulties of high-temperature electronic packaging, long-term high-temperature testing of ohmic contacts has to date been carried out without current flowing through the contact. Electromigration and chemical reactions driven by electrical bias in a 300 °C–600 °C oxidizing environment that could negatively impact wide bandgap ohmic contact reliability have yet to be studied. Therefore, substantial challenges remain to be overcome before wide bandgap contacts are ready to support prolonged (years) of operation in air at ambient temperatures near 600 °C.

### C. Packaging

The unavailability of a mature packaging technology for 300 °C–600 °C operation partially hinders development and demonstration of electronic devices for this temperature range. The major challenges to realizing such a packaging technology are chemical, physical, and electrical stability of both the packaging materials themselves as well as the interfaces between these materials. Most metals and alloys, including some noble metals, undesirably oxidize at temperatures approaching 500 °C when atmospheric oxygen is present. Therefore, most metals and alloys commonly used in conventional IC packaging, such as Cu, Al, and Au/Ni-coated Kovar, would not be practical for this environment, unless they are maintained in a perfectly hermetically sealed inert/vacuum environment by the rest of the package. If more than one metallic material is used in an electrical connection, in some cases undesirable intermetallic phases may form at interface of different metals, such as Al and Cu, at high temperatures. These intermetallic phases often reduce the mechanical strength of an interconnnection system.

As the part is thermally cycled, the large temperature range encountered (−55 °C–600 °C) increases stress caused by mismatch in the coefficient of thermal expansion (CTE) between different materials in the package. CTE mismatch between the die, die-bond material, and the package baseplate will place stress on the wide bandgap die itself. Therefore, to minimize stress, the CTE of all materials in the die-attach should be matched as best as possible. In cases where a backside electrical contact is required, the die-bonding material must be chemically and electrically compatible with the wafer backside metallization. The requirement of CTE match at package seals restricts the sealing material selection in order to ensure hermeticity under thermal cycling. Besides the CTE match requirement for obtaining a hermetic

seal that would withstand thermal cycling, high temperatures significantly promote thermal processes such as diffusion and degassing at material surfaces that would likely lead to contamination of the hermetic cavity atmosphere over time. Achieving and verifying hermetic seal for long-term 300 °C–600 °C operation will be challenging.

In order to realize practical high-temperature electronics packaging, innovative packaging materials and package designs concepts are required. Recently, aluminum nitride (AlN) insulating noncrystalline ceramic, which has CTE properties very close to SiC, was proposed as substrate material for high-temperature device packaging [42], [43]. Thick-film materials appear promising for use as substrate metallization in realizing 500 °C hybrid packaging [44]. A gold thick-film metallization on AlN ceramic-based 500 °C packaging for SiC devices has been demonstrated [45]. The electrical interconnection system of this approach has been tested in an air environment for over 5000 h at 500 °C and a packaged SiC test device operated for over 1000 h. High-temperature passive components, such as inductors, capacitors, and transformers, must also be developed for operation in demanding conditions before the full system-level benefits of high ambient temperature power electronics can be successfully realized.

### *D. High-Temperature Device Technology*

The availability of ohmic contacts, interconnects, and packaging that could function over an acceptable time period at $T = 300$ °C–600 °C could permit initial realization of some useful wide bandgap devices and circuits. In the early days of silicon electronics before the MOSFET was sufficiently developed and reliable (1960s), device structures constructed only of p-n junctions and metal-semiconductor junctions were employed to realize discrete transistors and smaller scale ICs. Examples of such junction devices are BJTs, junction FETs, and metal–semiconductor FETs (MESFETs) [9]. While the MOSFET best accomplishes most of today's room-temperature application requirements, there are nevertheless commercially viable VLSI circuits are realized using silicon BJTs and GaAs MESFETs, as well as discrete power p-n junction rectifiers and thyristors. Given sufficiently reliable contacts, packaging, and interconnect, SiC and/or GaN versions of these junction-device approaches could be used to achieve $T = 300$ °C–600 °C wide bandgap discretes and ICs. However, a potential major impediment to realizing this vision in many applications is the presence of charge-trapping effects in SiC and GaN that undesirably change device electrical characteristics as a function of temperature and applied bias. This important issue that can also impact wide bandgap devices operating at room temperature ambient is detailed in [65]. Robust circuit designs that accommodate large changes in device operating parameters will also be necessary for designing wide temperature range (as large as 655 °C spread) circuit functionality.

While junction devices can provide useful high-temperature functionality, insulated-gate FETs (IGFETs), such as the silicon MOSFET depicted in Fig. 2, are nevertheless preferred for practical circuit design and implementation. In order to implement an insulated gate transistor that can operate at $T = 300$ °C–600 °C for long time periods, a gate-insulator material that maintains good insulating and interfacial properties under high-temperature and high electric field stress must be developed. Unfortunately, obtaining such behavior from gate insulators on wide bandgap semiconductors has proven extremely problematic to date.

More technology-specific issues associated with poor wide bandgap IGFET performance are addressed in [60] and [61]. As discussed in these papers, the vast majority of IGFET devices in SiC have been implemented using thermally grown oxide and/or nitride dielectrics. In contrast, gate insulators in III-N IGFETs are often epitaxially grown AlGaN alloys. While both SiC and III-N IGFETs have demonstrated brief operation in above 600 °C [46], [47], viable long-term operation at high ambient temperatures will require further substantial improvements in gate-insulator capability. In broad terms, there are two primary areas where gate insulators employed wide bandgap transistors are generally deficient relative to the demanding requirements needed for successful high ambient temperature operation. First, the insulating properties are often insufficient, allowing charge to undesirably leak from the transistor channel. This charge can create and/or occupy traps in the insulator, resulting in undesirable changes the threshold voltage ($V_T$) of the IGFET over time. Given the thermally activated nature of insulator carrier leakage and degradation mechanisms, both of these deficiencies get considerably worse with increasing operating temperature [33], [48]–[54]. Second, the densities of undesirable electronic charge states near the semiconductor/insulator interface have been much higher for wide bandgap devices than for silicon devices. The states contribute to poor effective channel mobility ($\mu$) that greatly harms the IGFET electrical performance [11], [55], [56].

Research efforts aimed at realizing improved wide bandgap IGFETs, primarily based on alternative processing methods and/or gate-insulator materials, have yielded measurable progress [47], [56]–[59]. Nevertheless, wide bandgap IGFET channel and gate-insulator properties remain substantially inferior in performance and reliability compared to $Si/SiO_2$ MOSFETs, even for operation near room temperature. Therefore, formidable developmental challenges remain to be overcome before wide bandgap IGFETs that offer acceptable performance and reliability at operational temperatures well beyond 300 °C become attainable.

## IV. Summary

While high-temperature wide bandgap semiconductor electronics can be classified as a niche market technology, it nevertheless will offer important capabilities to automotive, aerospace, energy production, and other industrial systems that will affect modern everyday life. Wide bandgap semiconductors will be used in high-temperature application

needs that cannot be met with more readily available technologies such as SOI. Significant technology challenges remain to be overcome for both SiC and GaN, but SiC appears closer to beneficial high ambient temperature functionality than GaN. As discussed here and in other papers in this Special Issue of the PROCEEDINGS OF THE IEEE, significant progress continues to be made toward overcoming these challenges. Since the theoretical high-power switching properties of the wide bandgaps is unmatched at all temperatures, wide bandgap semiconductor power devices will play a significant role in realizing beneficial high ambient temperature power conditioning circuits. For low-power circuits, wide bandgap electronics will likely be relegated to the temperature range beyond the reach of SOI electronics, which appears to be above 300 °C.

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